An Integrated Reconfigurable SAW-Less Quadrature Balanced N-Path Transceiver for Frequency-Division and Half Duplex Wireless

Erez Zolkov, Nimrod Ginzberg, Emanuel Cohen
Faculty of Electrical Engineering, Technion, Israel

***Abstract*— In this work, we propose a fully integrated transceiver for frequency-division and half duplex wireless operation based on a quadrature balanced N-path mixer-first architecture. The quadrature balanced N-path transceiver (QBNT) comprises a quadrature hybrid and two identical mixer-first receivers (MFRXs), presenting a short circuit and 50 ohms matching in the transceiver (TX) and receiver (RX) bands, respectively. The TX power reflects at the MFRXs' interface and adds up in-phase at the antenna, while the RX signal from the antenna is reconstructed in phase in digital baseband, with the TX noise cancelled at RX regardless of antenna voltage standing wave ratio. QBNT equations and design considerations are shown. An integrated QBNT prototype was fabricated in TSMC 65nm CMOS process as a proof of concept, occupying an active area of 2.96 mm^2. The QBNT operates at the frequency range between 0.75-2 GHz with a TX-RX offset above 200 MHz. It achieves RX noise figure (NF) of 2.8-5.8 dB, RXB1dB of 18 dBm, TX-ANT OIP3 of 27.3 dBm and 29.5 dBm in FDD and half duplex (HD) modes, respectively. The RX and TX (at OP1dB) consume DC power of 82-130 mW and 254 mW, respectively.**

***Keywords*— Full-Duplex (FD), Frequency Division Duplex (FDD), Interference Cancellation, Quadrature Balanced LNAs (QBLNA), Quadrature Balanced N-path Transceiver (QBNT), N-path Mixer, Mixer-First Receiver.**

I. Introduction

Frequency division duplexing (FDD) offers reduced latency and greater coverage relative to time division duplexing (TDD) and is used in many licensed bands for cellular communications worldwide [1]. Currently, most FDD communication systems employ external bulky filters that are expensive and consume a substantial area. Recent integrated single-antenna FDD works with embedded duplexing capabilities have leveraged self-interference cancellation (SIC) techniques to perform on-chip filtering. [2] presents an active cancellation approach that achieves operation in relatively small transmitter (TX)-receiver (RX) offset, but draws substantial power and degrades the RX's noise figure (NF). In [3], an electrical balance duplexer (EBD) is used to provide passive TX-RX isolation at the cost of 3 dB loss in both TX and RX paths. [4] presents a highly integrated FDD transceiver implemented by employing distributed power amplifiers (PA) and offers wide operational frequency range, at the cost of high RX NF and narrowband SIC. Moreover, the above techniques are sensitive to antenna voltage standing wave ratio (VSWR) variations, and usually require radio frequency (RF) calibration with inherent bandwidth (BW) and channel delay limitations.

In this work, we propose a fully integrated FDD transceiver based on quadrature balanced N-path mixer-first receivers (MFRX). The quadrature balanced N-path transceiver (QBNT, Fig. 1) offers reconfigurable and wideband built-in FDD duplexing and supports HD-TX operation mode as well. The QBNT integrates a PA, a quadrature hybrid, and two identical N-path-based MFRXs. The MFRXs outputs are combined in digital baseband (BB) using a BB algorithm that extracts the desired RX signal from the undesired TX signal and noise leakage. The proposed transceiver offers high TX power handling with low TX-to-antenna insertion loss (IL), while maintaining high RX sensitivity even in the presence of antenna VSWR.

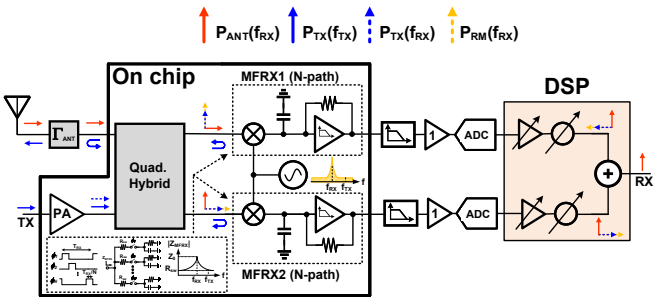


Fig. 1. The proposed QBNT, with its principle of operation.

II. Theory of Operation

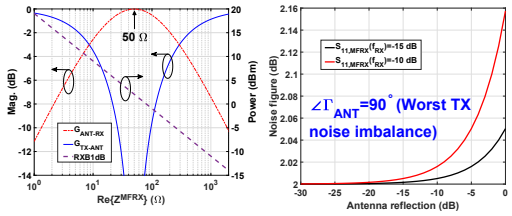
The QBNT principal of operation is as follows: In the RX band, the MFRXs show impedance matching, allowing constructive in-quadrature reception of the antenna RX and destructive in-quadrature interference of the PA noise signal by the digital BB algorithm. At the TX band, the MFRXs present low input impedance, causing the TX signal to reflect at the MFRXs interface and to reconstruct in-phase at the antenna.

The MFRX input impedance (Z_{MFRX}) design is an important part in the system's performance. Matching in MFRX is achieved by designing an adequate BB impedance that translates to ∼50 Ω at RF. The in-band (IB) antenna-RX gain is given by the IB return loss of the MFRX [5]:

$$G_{ANT-RX} = 1 - |S_{11,MFRX}(f_{RX})|^2 \quad (1)$$

On the other hand, the QBNT out-of-band (OOB) performance, namely at TX frequencies, depends on the MFRX impedance at OOB frequencies, which roughly equals to the MFRX's switches resistance. The RX OOB blocker 1dB compression point (RXB1dB) and TX-antenna (ANT) gain are given by [5]:

$$RXB_{1dB} = \frac{V_{max}^2}{2R_{sw}} \quad (2)$$



(a) (b)

Fig. 2. (a) QBNT performance vs. MFRX real input impedance and (b) RX NF vs. antenna reflection, in the case of maximum TX noise imbalance, for various MFRX return losses.

$$G_{TX-ANT} = S_{11,MFRX}(f_{TX}) = \frac{R_{sw} - Z_0}{R_{sw} + Z_0} \qquad (3)$$

Where V_{max} is a process and input bias related parameter. Equations (2,3) show that high RXB1dB and low TX-ANT insertion loss (IL) can be achieved by implementing large switches with low ON resistance, trading off linearity and IL with power consumption and frequency tuning range [6]. This claim is verified in Fig. 2a, which plots the above equations vs. the MFRX input impedance, assuming it is purely real.

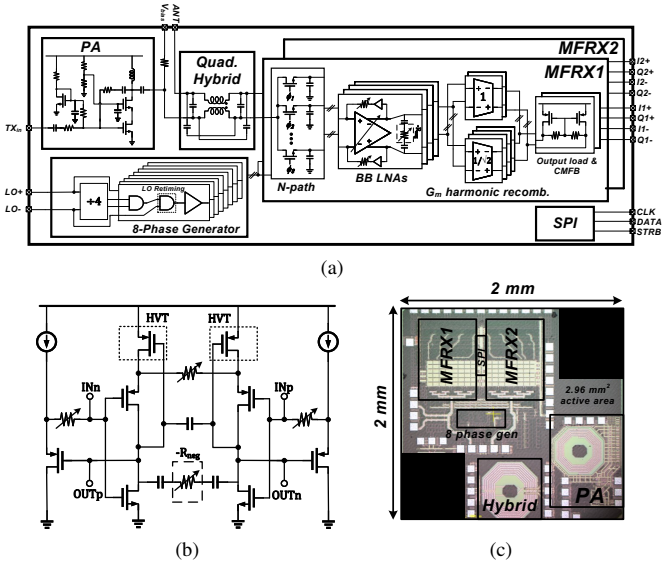
Both TX noise and TX-induced reciprocal mixing (RM) are absorbed by the MFRXs due to their ∼50 ohms matching at RX frequencies, and are removed digitally in BB since they both appear out-of-phase at both MFRXs outputs, in contrary to the RX signals which appear in-phase. This means that barely any TX noise and RM reflect from the MFRXs to the antenna, leading to a minor VSWR impact on RX NF, even for realistic MFRX matching. Furthermore, amplitude and phase mismatches between the two RX paths are corrected digitally with negligible effect on RX NF. This claim is shown in Fig. 2b [5], where the theoretical RX NF is plotted assuming NF_{MFRX}=2 dB and 90° TX noise reflection, leading to maximum TX noise amplitude imbalance at the two MFRXs inputs. We see that even for -10 dB RX matching there is less than 0.2 dB RX NF degradation.

A. System Calibration Procedure

Channel estimation is performed digitally to combine the two MFRXs' outputs for optimal TX noise cancellation. For the system calibration, an OFDM calibration signal which BW is equal to the RX BW is transmitted through the TX port solely. The signal is recorded at all four IQ outputs of the RX, and an IQ correction algorithm is applied to each MFRX's IQ output for recombination. Then, channel estimation is performed to estimate the transfer function (TF) between the TX port to each MFRX output. We denote MFRX1 and MFRX2 output signals $MFRX1(f)$ and $MFRX2(f)$, respectively, and the TF between the ANT port to MFRX1 and MFRX2 outputs as $H_1(f)$ and $H_2(f)$, respectively. Finally, the RX output is obtained by subtracting both MFRXs' outputs divided by their respective TFs, meaning that $RX(f) = MFRX1(f)/H_1(f) - MFRX2(f)/H_2(f)$.

III. Implementation

We have implemented the QBNT system in a TSMC 65nm CMOS process. The chip schematic is shown in Fig. 3a, and



(a) (b) (c)

Fig. 3. (a) QBNT chip schematic, (b) BB LNA schematic and (c) QBNT chip micrograph.

its micrograph is shown in Fig .3c. The QBNT occupies an active area of 2.96 mm^2 and consumes 336-384 mW for full FDD operation at TX OP1dB, at a frequency range of 0.75-2 GHz. Each MFRX operates from a 1.2 V supply (except for the N-path switches' drivers which operate from 1.5 V supply for higher switches linearity) and occupies an active area of 0.29 mm^2. The MFRX includes an N-path filter with 8 phases, whose switches were sized to provide ON resistance of 3 Ω for OOB S_{11} lower than -1 dB, resulting in theoretical <1 dB TX-ANT IL (Fig. 2a). The N-path filter is followed by 4 reactance-cancelling BB LNAs (Fig. 3b), which provide wideband matching [7] without degrading the OOB rejection and achieve 40 dB/dec BB filtering, by exploiting the BW limited negative capacitance achieved by the BB LNA's resistive feedback and its low-pass response. The BW and gain of the LNAs are set by a tunable degeneration resistor and a tunable negative resistance at the LNAs outputs. The resistive feedback is achieved by buffering the LNAs outputs using source followers. In this work, we have set the LNA BW so that the overall MFRX BW will be equal to 20 MHz. The 8 BB LNAs outputs are recombined to differential I/Q outputs using 1 and $1/\sqrt{2}$ Gm-weighted stages [8] sharing two output loads. The MFRX also supports low input impedance (Low Z) mode for HD-TX operation, at which all 8 switches are turned ON to provide lower input impedance of 3/8 Ω, resulting in higher reflectivity and lower TX-ANT IL. The BB outputs of the chip are connected to external discrete ADA4897 amplifiers for differential-to-single conversion, and output 50 ohms matching, with closed loop gain of G=1. An 8-phase generator drives the MFRXs for phase noise (PN) correlation and is composed by a differential divide-by-4 circuit, followed by logic circuits that generate 8 clock phases with a 25% duty cycle. The clock phases are retimed (ANDed) with the input LO clocks to generate 12.5% duty cycle non-overlapping pulses, such that their phase noise is dictated by the clean

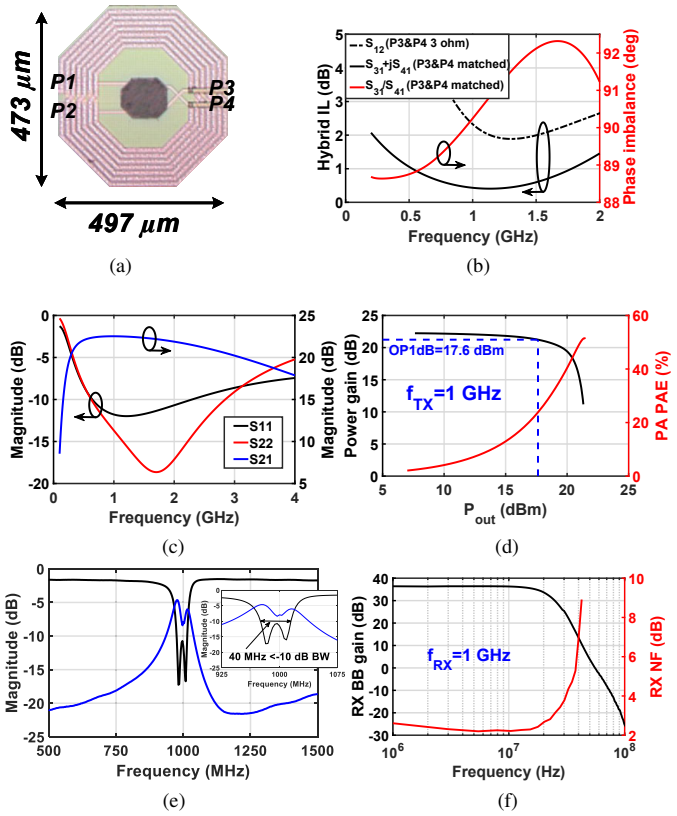


Fig. 4. (a) Quadrature hybrid layout, and measured standalone QBNT blocks performance of: (b) quadrature hybrid IL and phase imbalance, (c) PA S-parameters, (d) PA gain and PAE vs. P_{out}, (e) MFRX RF gain and matching at LO frequency of 1 GHz and (f) MFRX BB gain and NF at LO frequency of 1 GHz.

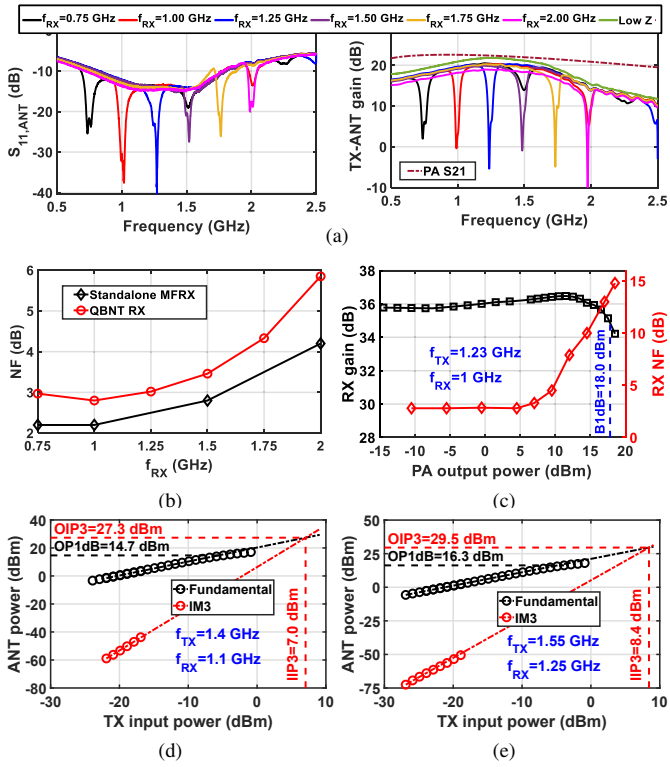


Fig. 5. QBNT CW measurements of: (a) Antenna matching and TX-ANT gain vs. frequency for different LO frequencies, (b) NF vs. LO frequency, (c) RX voltage gain and NF vs. TX output power, as f_{TX}= 1.23 GHz and f_{RX}=1 GHz, (d) TX-ANT FDD IM3 measurement as f_{TX} =1.4 GHz and f_{RX}=1.1 GHz, and (e) TX-ANT HD IM3 measurement as f_{TX} =1.55 GHz and f_{RX}=1.25 GHz

reference LO rather than by the PN of the divider circuitry [8]. Simulations show that the internal drivers' PN, assuming ideal LO, is -175 dBc/Hz at frequency offsets of >100 MHz.

The PA topology is a Class-B biased cascode with resistive shunt-shunt feedback, operating from a 3.3 V supply and occupying an area of 0.49 mm^2. To achieve wideband response, we combined simultaneous input and output matching through the feedback resistor and the cascode's transconductance gain and selected $R_{opt} \approx$ 50 ohms. The quadrature hybrid consists of two coupled inductors and shunt capacitors, with a moderate area of 0.497×0.473 mm^2 (Fig. 4a). To extend the operational BW, feedforward cross-coupled capacitors between diagonal ports were employed [9].

IV. Measurements

A. *Continuous wave measurements*

To characterize each QBNT block independently, we have measured the chip die using a probe station. The quadrature hybrid achieves better than -15 dB port matching and port isolation between 0.5-2 GHz, and less than 1 dB IL ($S_{31} + jS_{41}$) between 0.5-1.75 GHz with <2.5° phase imbalance across the entire band (Fig. 4b). Measurements show a <2 dB TX-ANT IL (S_{12}) between 1-1.5 GHz when ports 3 and 4 are terminated with 3 ohms, to represent the OOB MFRX input impedance. The PA continuous wave (CW) measurements are presented in Fig. 4c at the frequency range of 0.75-2 GHz, showing a small signal gain of 21-22.5 dB and <-10 dB matching at both input and outputs ports. An output power 1dB gain compression point (OP1dB) of 17.6 dBm and peak power added efficiency (PAE) of 51% are achieved at an input frequency of 1 GHz (Fig. 4d). The MFRX has wideband <-10 dB matching across the BW of 40 MHz with a band-pass RF gain centred around the LO (Fig. 4e). Fig. 4f shows the MFRX BB response at 1 GHz LO. The RX BB BW is 20 MHz with a DC gain of 36 dB and 80 dB/dec OOB filtering slope (40 dB/dec from ext. board filtering), and the IB NF is 2.2-2.7 dB. For the QBNT system measurements, wire-bonds were used to connect between the different blocks, and the chip die was mounted on an FR4 PCB (Fig. 6a). Fig. 5a shows the QBNT S-parameters measurement results. The antenna port exhibits <-15 dB matching in the RX band, while the TX-ANT gain has 2 dB and 0.8 dB IL at FDD and HD modes, respectively, relative to the standalone PA gain (Fig. 4c), and a notch at the RX frequency (in FDD mode), owing to the MFRXs' matching at RX band. Standalone MFRX and QBNT RX (measured assuming ideal channel summation) NF are between 2.2-4.1 dB and 2.8-5.85 dB, respectively (Fig. 5b). The RX gain is 36 dB, with B_{1dB} of 18 dBm, achieved by the low switches' resistance and the MFRXs input bias point [3], combined

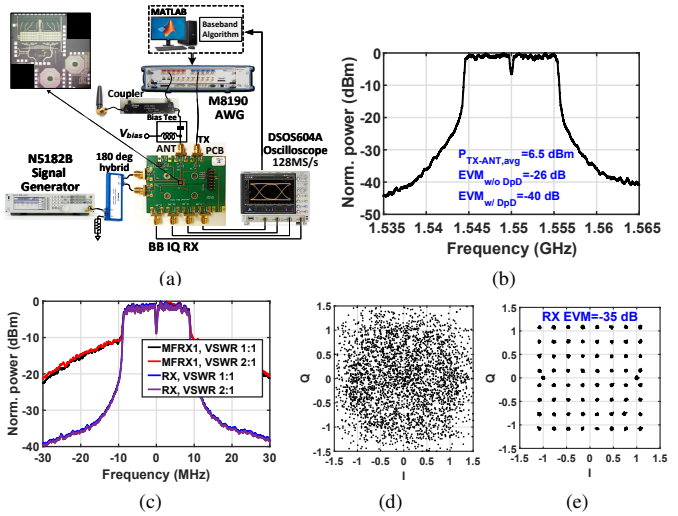


Fig. 6. (a) FDD dynamic measurements setup, (b) antenna TX spectrum, (c) RX spectrum, (d) EVM of a single MFRX channel and (e) EVM of the reconstructed RX signal.

with the PA's power split between the two MFRXs with additional IL of about 0.5 dB (Fig. 5c). Blocker noise figure (BNF) measurements, that were performed without filtering the external LO show 1 dB NF degradation for a PA output power of 8 dBm. We see that the RM induced by the external LO PN (measured to be -160 dBc/Hz) is cancelled, and the NF degradation is attributed to the internal PN. For example, at PA output power of 15 dBm the RXNF is 11 dB, which fits the -175 dBc/Hz PN along with the 3 dB hybrid power split. TX-ANT FDD and HD large signal measurements are shown in Fig. 5d and 5e, respectively, showing an OP1dB of 14.7 dBm in FDD mode and 16.3 dBm in HD mode.

B. Dynamic measurements

The dynamic measurements setup is shown in Fig. 6a. For these measurements, we have transmitted 20 MHz OFDM Wi-Fi signals at both the TX and ANT ports. The transmitted TX signal's average power was chosen to be 8.5 dBm (resulting in 6.5 dBm TX power at the ANT port-Fig. 6b), which corresponds to a 9.5 dB back-off from the RX B1dB, to avoid RX EVM degradation caused by TX cross-modulation. Higher TX power can be supported by employing an RX post-distortion algorithm [10]. To account for the non-linearity of the PA and the MFRXs' switches, we applied a digital pre-distortion (DPD) to the TX signal, using a memoryless 4th order polynomial, leading to an EVM improvement from -26 dB to -40 dB. For RX measurements, we have transmitted an ANT signal in RX band with power of -40 dBm, and a TX signal that includes noise in the RX band. To extract the RX signal at BB, we have followed the algorithm the described in section II-A for each VSWR configuration. Spectrum measurements (Fig. 6c) show wideband TX noise cancellation in the reconstructed RX output. Constellations of MFRX1 (Fig. 6d), which stands for a single MFRX output before channel summation, and RX output (Fig. 6e) for antenna VSWR of 2:1 indicate significant noise cancellation upon RX channels recombination with an RX EVM of -35 dB.

Table 1. Comparison to prior art

Features	JSSC 17' [2]	JSSC 18' [3]	JSSC 17' [4]	This work
Architecture	Cancellation DAC	EBD&N-path LNA	Distributed transceiver	QBNT
Technology	CMOS 65 nm	CMOS 180 nm SOI	CMOS 65 nm	CMOS 65 nm
f_{RF} (GHz)	1-1.8	0.7-1	0.3-1.5	0.75-2
TX-RX frequency offset (MHz)	40	0-300	>100	>200
RX gain (dB)	18	4.8-5.5	24-32	36
ANT-RX NF (dB)	7.6	9[a]	7-12	2.8-5.8
TX-ANT IL (dB)	3.3 (FDD) 0.35 (HD)	2.9-3.6 (FDD)	3-5 (FDD)	2 (FDD[b]) 0.8 (HD[b])
RX BW (MHz)	N/R	3.8	N/R	40
IB ANT-RX IIP3 (dBm)	N/R	6.4[a]	N/R	-8
RX $B_{1dB}/\Delta f$ (dBm/MHz)	12.6/40	23/40 ($\frac{\Delta f}{BW}$=10.5)	13/125	18/230 ($\frac{\Delta f}{BW}$=5.7)
TX-ANT OIP3 (dBm)	25	N/A (no PA)	N/R	27.3 (FDD) 29.5 (HD)
TX-ANT P_{sat} (dBm)	16 (FDD) 18.8 (HD)	N/A (no PA)	26 (FDD) 20 (TDD)	19.5 (FDD) 20.5 (HD)
Power (mW)	RX&LO:40 PA:180 DAC:60	RX and LO:62.5	RX:100 PA:600 RX-LO:N/R	RX:38[c] PA:254 RX-LO:44-92
Active area (mm^2)	3.9	9.62	7.2	2.96

[a] RX at RF with LNA [b] At TX frequency range of 1.1-1.5 GHz
[c] Excluding external board buffers N/R: Not reported N/A: Not applicable

V. Conclusion

In this work we have presented a fully integrated single-antenna FDD diplexer-transceiver with antenna VSWR and blocker resilience. Principle of operation and design equations were discussed. Implementation in TSMC 65 nm CMOS process is shown. Measurement results achieve low RX NF and TX-ANT IL, high TX-ANT P_{SAT} and OIP3 with compact die size comparing to prior art (Table 1).

References

[1] Pooya Monajemi and Brian Hart, "STR Capability Report", IEEE 802.11-20/0809r0.
[2] L. Calderin et al., "Analysis and Design of Integrated Active Cancellation Transceiver for Frequency Division Duplex Systems," in JSSC, vol. 52, no. 8, pp. 2038-2054, Aug. 2017.
[3] G. Qi et al., "A SAW-less tunable RF front end for FDD and IBFD combining an electrical-balance duplexer and a switched-LC N-path LNA," JSSC, vol. 53, no. 5, pp. 1431–1442, May 2018.
[4] H. Yüksel et al., "A Wideband Fully Integrated Software-Defined Transceiver for FDD and TDD Operation," in JSSC, vol. 52, no. 5, pp. 1274-1285, May 2017.
[5] E. Zolkov et al., "A 1-2-GHz Quadrature Balanced N-Path Receiver for Frequency Division Duplex Systems," in TMTT.
[6] D. Yang et al., "Optimized Design of N-Phase Passive Mixer-First Receivers in Wideband Operation," in TCAS I, vol. 62, no. 11, pp. 2759-2770, Nov. 2015.
[7] E. Zolkov and E. Cohen, "A Mixer-First Receiver With Enhanced Matching Bandwidth by Using Baseband Reactance-Canceling LNA," in SSCL, vol. 4, pp. 109-112, 2021.
[8] C. Andrews and A. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable RF interface," in JSSC, vol. 45, no. 12, pp. 2696–2708, Dec. 2010.
[9] J. S. Park and H. Wang, "A Transformer-Based Poly-Phase Network for Ultra-Broadband Quadrature Signal Generation," in TMTT, vol. 63, no. 12, pp. 4444-4457, Dec. 2015.
[10] N. Ginzberg et al., "A Tunable Multimode Quadrature Balanced N-Path Diplexer With Nonlinear Cross-Modulation Distortion Correction," in MWCL, vol. 31, no. 6, pp. 646-649, June 2021.